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(54) **ARRAY SUBSTRATE, MANUFACTURING METHOD THEREOF AND DISPLAY PANEL**

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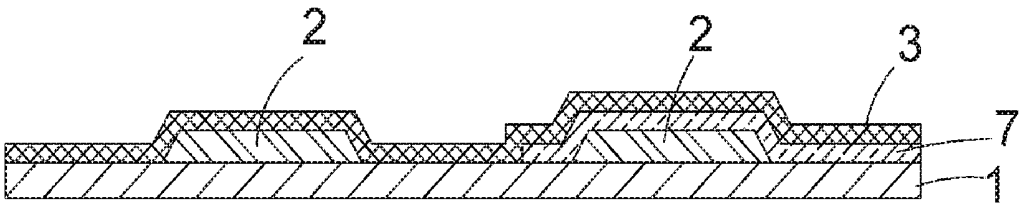
(57) **ABSTRACT**

An array substrate is provided, including a substrate, a driver thin film transistor and a switch thin film transistor disposed on the substrate, the driver thin film transistor and the switch thin film transistor both include a gate, a gate insulating layer, an active layer, a source, and a drain. A barrier layer is disposed between the gate and the gate insulating layer of the driver thin film transistor. A manufacturing method thereof includes forming a barrier layer on the gate of the driver thin film transistor. Compared with existing arts, forming a barrier layer between the gate and the gate insulating layer of the driver thin film transistor to prevent its active layer from water and active oxygen ions affections can improve the electrical property and reliability of the thin film transistor, and ensure the normal operation for driving the driver thin film transistor of organic light emitting diode.



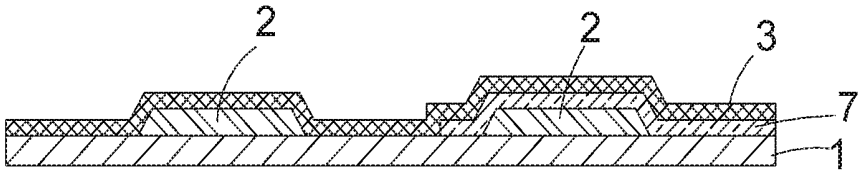


FIG. 1

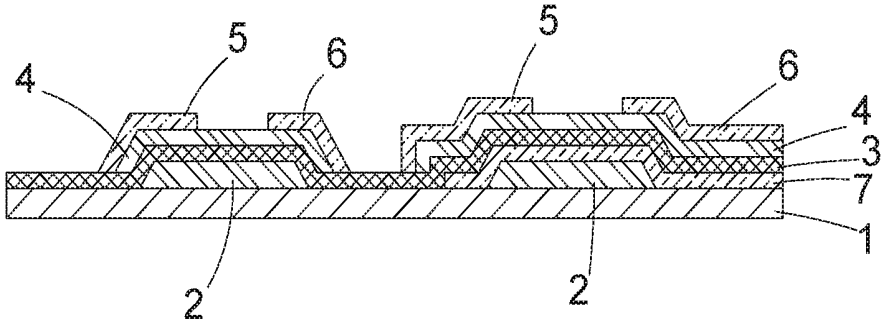


FIG. 2

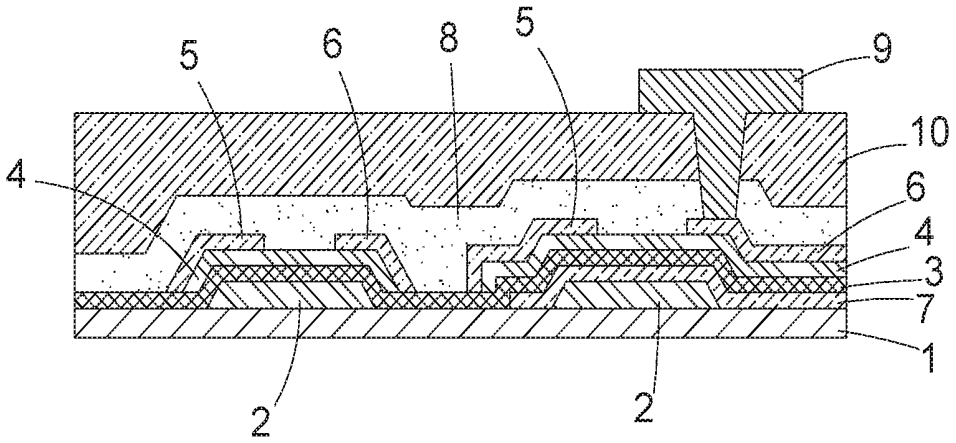


FIG. 3

ARRAY SUBSTRATE, MANUFACTURING METHOD THEREOF AND DISPLAY PANEL

RELATED APPLICATIONS

[0001] The present application is a National Phase of International Application Number PCT/CN2017/099484, filed Aug. 29, 2017, and claims the priority of China Application No. 201710584353.4, filed Jul. 18, 2017.

FIELD OF THE DISCLOSURE

[0002] The present disclosure relates to a display panel technology, and more particularly to an OLED array substrate, a manufacturing method thereof, and a display panel.

BACKGROUND

[0003] As organic light emitting diode (OLED) panels are gaining popularity, their thickness is thinner relative to LCD panels due to the absence of additional back light components. Wherein indium gallium zinc oxide (IGZO) in metal oxide semiconductors, due to the advantages of high electron mobility, low current leakage, and low preparation temperature, have aroused widespread concern.

[0004] In the conventional bottom gate type IGZO thin film transistor, during the process of manufacturing, the gate insulating layer at the switch thin film transistor (Switch TFT) and the driver thin film transistor (Driver TFT) generally adopts SiOx material. However, the hydrophilicity of SiOx is relatively strong and has a strong ability to absorb water and oxygen at room temperature. After the TFT works for a certain period, the electrical properties of the TFT will be seriously affected, resulting in a large shift of the threshold voltage, the reliability becomes poor, and TFT properties are serious deteriorated.

SUMMARY

[0005] In order to overcome the shortcomings of the prior arts, the present disclosure provides an array substrate, a manufacturing method thereof, and a display panel, for improving the typicality and reliability of the thin film transistor and ensuring the normal operation of the driver thin film transistor.

[0006] The present disclosure provides an array substrate, comprises a substrate. A driver thin film transistor and a switch thin film transistor are disposed on the substrate. The driver thin film transistor and the switch thin film transistor both comprise a gate, a gate insulating layer, an active layer, a source, and a drain. A barrier layer is further disposed between the gate and the gate insulating layer of the driver thin film transistor.

[0007] Furthermore, a material of the barrier layer is SiNx.

[0008] Furthermore, the active layer is an oxide thin film transistor, and/or the driver thin film transistor and the switch thin film transistor is a bottom-gate thin film transistor.

[0009] Furthermore, the array substrate further comprises a passivation layer and a planarization layer disposed over the driver thin film transistor and the switch thin film transistor. An anode is connecting to the source and the drain of the driver thin film transistor via via holes of the planarization layer and the passivation layer.

[0010] The present disclosure further provides a method of manufacturing an array substrate, comprising the steps of:

[0011] Step S1, patterning a gate layer prepared on the substrate to obtain gates of the driver thin film transistor and the switch thin film transistor.

[0012] Step S2, forming a barrier layer on the gate of the driver thin film transistor;

[0013] Step S3, depositing a gate insulating layer on the substrate.

[0014] Step S4, forming an active layer on the gate insulating layer above the gates of the driver thin film transistor and the switch thin film transistor.

[0015] Step S5, fabricating a source and a drain on the active layer.

[0016] Furthermore, the step S2 of forming a barrier layer on the gate of the driver thin film transistor particularly comprises: pattering a SiNx layer deposited on the gate of the driver thin film transistor by a plasma enhanced chemical vapor deposition process to obtain the barrier layer.

[0017] Furthermore, the active layer is an oxide thin film transistor.

[0018] Furthermore, the driver thin film transistor and the switch thin film transistor are bottom-gate thin film transistors.

[0019] Furthermore, the method of manufacturing an array substrate further comprises:

[0020] Step S6, forming a passivation layer on the substrate, the passivation layer covering the source and the drain.

[0021] Step S7, fabricating a planarization layer on the passivation layer.

[0022] Step S8, forming an anode on the planarization layer, the anode connecting to the source and the drain of the driver thin film transistor via via holes of the planarization layer and the passivation layer.

[0023] The present disclosure further provides a display panel, comprising the foregoing array substrate.

[0024] Compared with the existing arts, by providing a barrier layer between the gate and the gate insulating layer of the driver thin film transistor to prevent the active layer of the driver thin film transistor from water and active oxygen ions affections can improve the electrical property and reliability of the thin film transistor, and ensure the normal operation for driving the driver thin film transistor of organic light emitting diode.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] FIG. **1** is a schematic structural view of fabricating a barrier layer and a gate insulating layer of the present disclosure;

[0026] FIG. **2** is a schematic structural view of fabricating an active layer, a source and a drain on the gate insulating layer of the present disclosure;

[0027] FIG. **3** is a schematic structural view after fabricating a passivation layer, a planarization layer and an anode of the present disclosure.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0028] The present disclosure will be further described in the following description with reference to the accompanying drawings and embodiments.

[0029] As shown in FIG. **3**, an array substrate provide by the present disclosure is applied on OLED panel. The array substrate comprises a substrate **1**, a driver thin film transistor

and a switch thin film transistor are disposed on the substrate. Specifically, the driver thin film transistor and the switch thin film transistor both comprise a gate **2**, a gate insulating layer **3**, an active layer **4**, a source **5**, and a drain **6**. A barrier layer **7** is further disposed between the gate **2** and the gate insulating layer **3** of the driver thin film transistor. A passivation layer **8** is disposed over the driver thin film transistor and the switch thin film transistor above the source **5** and the drain **6**, a planarization layer **10** is disposed on the passivation layer **8**. An anode **9** connecting to the source **5** and the drain **6** of the driver thin film transistor via via holes of the planarization layer **10** and the passivation layer **8**.

[0030] By providing the barrier layer **7** between the gate **2** and the gate insulating layer **3** of the driver thin film transistor to prevent the active layer of the driver thin film transistor from water and active oxygen ions affections can improve the electrical property and reliability of the thin film transistor, and ensure the normal operation for driving the driver thin film transistor of organic light emitting diode.

[0031] The material of the barrier layer **7** is Silicon Nitride (SiNx). Since the hydrophilic of SiNx is much smaller than SiOx, which used as the material of the gate insulating layer **3**, it is capable of blocking water, oxygen, and impurity ions.

[0032] The active layer **4** of the present disclosure is an oxide thin film transistor, in particularly, is a metal oxide thin film transistor. In one embodiment of the present disclosure, the active layer **4** is Indium Gallium Zinc Oxide (IGZO).

[0033] The driver thin film transistor and the switch thin film transistor are bottom-gate thin film transistors.

[0034] A method of manufacturing an array substrate according to the present disclosure comprises the following steps:

[0035] Step S1, as shown in FIG. **1**. Patterning a gate layer prepared on the substrate to obtain gates of the driver thin film transistor and the switch thin film transistor. Specifically, depositing a layer of Molybdenum (Mo) on the glass substrate **1** by a physical vapor deposition process, and then pattering the Mo layer to obtain the gate **2** of the driver thin film transistor and a switch thin film transistor.

[0036] Step S2, as shown in FIG. **1**. Forming a barrier layer **7** on the gate **2** of the driver thin film transistor. Specifically, depositing a SiNx layer on the gate **2** of the driver thin film transistor by a plasma enhanced chemical vapor deposition process, and then pattering the SiNx layer to obtain the barrier layer **7**.

[0037] Step S3, as shown in FIG. **1**. Depositing a gate insulating layer **3** on the substrate **1**, making the gate insulating layer **3** covering the barrier layer **7**. The depositing material of the gate insulating layer **3** is Silicon Oxide (SiOx).

[0038] Step S4, as shown in FIG. **2**. Forming an active layer **4** on the gate insulating layer **3** above the gates of the driver thin film transistor and the switch thin film transistor. Specifically, depositing an layer of IGZO by physical vapor deposition and then pattering the IGZO layer to obtain the active layer **4**. The active layer **4** is disposed on the gate **2** of the driver thin film transistor and the switch thin film transistor.

[0039] Step S5, as shown in FIG. **2**, Fabricating a source **5** and a drain **6** on the active layer **4**. Specifically, depositing a metal layer by physical vapor deposition, and then patterning the metal layer by a back channel etch process (BCE) to obtain the source **5** and the drain **6**.

[0040] Step S6, as shown in FIG. **3**. Forming a passivation layer **8** on the substrate **1**, the passivation layer **8** covers the source **5** and the drain **6**. Specifically, fabricating a SiOx layer on the source **5** and the drain **6** and then pattering the SiOx layer to obtain the passivation layer **8**. Fabricating via holes on the passivation layer **8** above the source **5** or the drain **6** of the driver thin film transistor. In particularly, fabricating a via hole above the drain **6**.

[0041] Step S7, as shown in FIG. **3**. Fabricating a planarization layer **10** on the passivation layer **8**. Specifically, fabricating an organic photoresist insulation and pattering the organic photoresist insulation to form the planarization layer **10**, and forming a via hole on the planarization layer **10** at the position of the via hole of the passivation layer **8**.

[0042] Step S8, as shown in FIG. **3**. Forming an anode **9** on the planarization layer **10**, the anode **9** is connecting to the source **5** and the drain **6** of the driver thin film transistor via via holes of the planarization layer **10** and the passivation layer **8**.

[0043] The driver thin film transistor and the switch thin film transistor of the present disclosure are bottom-gate thin film transistors.

[0044] The present disclosure further provides a display panel comprising the foregoing array substrate, which will not be repeated herein.

[0045] The array substrate of the present disclosure is particularly suitable for being applied in a thin film transistor backplane of an active-matrix organic light emitting diode (AMOLED).

[0046] While the disclosure has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the disclosure as defined by the appended claims and their equivalents.

What is claimed is:

1. An array substrate, comprising a substrate, wherein a driver thin film transistor and a switch thin film transistor are disposed on the substrate; the driver thin film transistor and the switch thin film transistor both comprise a gate, a gate insulating layer, an active layer, a source, and a drain; a barrier layer is further disposed between the gate and the gate insulating layer of the driver thin film transistor.

2. The array substrate according to claim **1**, wherein a material of the barrier layer is SiNx.

3. The array substrate according to claim **1**, wherein the active layer is an oxide thin film transistor, and/or the driver thin film transistor and the switch thin film transistor is a bottom-gate thin film transistor.

4. The array substrate according to claim **1**, further comprising a passivation layer and a planarization layer disposed over the driver thin film transistor and the switch thin film transistor, an anode connecting to the source and the drain of the driver thin film transistor via via holes of the planarization layer and the passivation layer.

5. A method of manufacturing an array substrate, comprising the steps of:

step S1, patterning a gate layer prepared on the substrate to obtain gates of the driver thin film transistor and the switch thin film transistor;

step S2, forming a barrier layer on the gate of the driver thin film transistor;

step S3, depositing a gate insulating layer on the substrate;

step S4, forming an active layer on the gate insulating layer above the gates of the driver thin film transistor and the switch thin film transistor;

step S5, fabricating a source and a drain on the active layer.

6. The method of manufacturing an array substrate according claim **5**, wherein the step S2 of forming a barrier layer on the gate of the driver thin film transistor particularly comprises: pattering a SiNx layer deposited on the gate of the driver thin film transistor by a plasma enhanced chemical vapor deposition process to obtain the barrier layer.

7. The method of manufacturing an array substrate according to claim **5**, wherein the active layer is an oxide thin film transistor.

8. The method of manufacturing an array substrate according to claim **7**, wherein the driver thin film transistor and the switch thin film transistor are bottom-gate thin film transistors.

9. The method of manufacturing an array substrate according to claim **5**, further comprising:

step S6, forming a passivation layer on the substrate, the passivation layer covering the source and the drain;

step S7, fabricating a planarization layer on the passivation layer;

step S8, forming an anode on the planarization layer, the anode connecting to the source and the drain of the driver thin film transistor via via holes of the planarization layer and the passivation layer.

10. A display panel, comprising an array substrate, the array substrate comprising a substrate, wherein a driver thin film transistor and a switch thin film transistor are disposed on the substrate; the driver thin film transistor and the switch thin film transistor both comprise a gate, a gate insulation layer, an active layer, a source and a drain; a barrier layer is further disposed between the gate and the gate insulating layer of the driver thin film transistor.

11. The display panel according to claim **10**, wherein a material of the barrier layer is SiNx.

12. The display panel according to claim **10**, wherein the active layer is an oxide thin film transistor, and/or the driver thin film transistor and the switch thin film transistor is a bottom-gate thin film transistor.

13. The display panel according to claim **10**, further comprising a passivation layer and a planarization layer disposed over the driver thin film transistor and the switch thin film transistor, an anode connecting to the source and the drain of the driver thin film transistor via though holes of the planarization layer and the passivation layer.

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专利名称(译)	阵列基板，其制造方法和显示面板		
公开(公告)号	US20190221626A1	公开(公告)日	2019-07-18
申请号	US15/578299	申请日	2017-08-29
[标]发明人	LI SONGSHAN		
发明人	LI, SONGSHAN		
IPC分类号	H01L27/32 H01L51/52 H01L51/56		
CPC分类号	H01L27/3262 H01L51/5237 H01L51/56 H01L27/3244 H01L27/326 H01L27/1225 H01L27/1237 H01L29/4908 H01L29/7869		
优先权	201710584353.4 2017-07-18 CN		
其他公开文献	US10692948		
外部链接	Espacenet USPTO		

摘要(译)

提供一种阵列基板，包括基板，驱动薄膜晶体管和设置在基板上的开关薄膜晶体管，驱动薄膜晶体管和开关薄膜晶体管均包括栅极，栅极绝缘层，有源层，来源和排水。阻挡层设置在驱动薄膜晶体管的栅极和栅极绝缘层之间。其制造方法包括在驱动器薄膜晶体管的栅极上形成阻挡层。与现有技术相比，在驱动薄膜晶体管的栅极和栅极绝缘层之间形成阻挡层，以防止其有源层受到水和活性氧离子的影响，可以改善薄膜晶体管的电性能和可靠性，并确保用于驱动有机发光二极管的驱动薄膜晶体管的正常操作。